What is claimed is:

1. A multi-threaded processor, comprising:

a processing pipeline including a number of stages, each stage processing at least one instruction, each instruction belonging to one of a plurality of threads; and

a fetch unit forming one of the stages of the pipeline and determining from which thread to fetch an instruction for processing by the processing pipeline, the fetch unit receiving information from at least one other stage of the processing pipeline and determining a processing time of the processing pipeline occupied by each thread based on the received information, the fetch unit determining from which thread to fetch an instruction for processing by the processing pipeline based on the determined processing time for each thread.

2. The processor of claim 1, wherein the fetch unit determines the thread having the smallest determined processing time as the thread from which to fetch an instruction for processing.

3. The processor of claim 1, wherein the received information includes the operation type of instructions in the processing pipeline.

4. The processor of claim 3, wherein the received information further includes the operation type of instructions leaving the processing pipeline.

5. The processor of claim 4, wherein the fetch unit includes a counter associated with each thread, each counter being incremented by a processing time associated with each instruction of the associated thread in the processing pipeline and being decremented by a processing time associated with each instruction of the associated thread leaving the processing pipeline.

6. The processor of claim 5, wherein the fetch unit determines the thread associated with the counter having a smallest count value as the thread from which to fetch an instruction for processing.

7. The processor of claim 1, wherein the fetch unit generates a weighted instruction count for each thread as the determined processing time of each thread, the weighted instruction count for a thread is a count of the instructions for the thread in the processing pipeline with each instruction weighted by the cycle counts associated with processing the instruction.

8. The processor of claim 7, wherein the fetch unit includes a counter associated with each thread, each counter being incremented by the cycle

counts associated with each instruction of the associated thread in the processing pipeline and being decremented by the cycle counts associated with each instruction of the associated thread leaving the processing pipeline.

9. The processor of claim 8, wherein the fetch unit determines the thread associated with the counter having a smallest count value as the thread from which to fetch an instruction for processing.

10. The processor of claim 1, wherein the processing pipeline comprises:

an instruction decoder decoding instructions, which the fetch unit determines to fetch, to generate at least an operation type of the instruction as decoder information; and

a queue storing the decoded instructions and issuing decoded instructions to an execution unit for execution.

11. The processor of claim 10, wherein the received information is the decoder information and the issued decoded instructions.

12. The processor of claim 1, wherein the processing pipeline further comprises:

an instruction cache storing instructions, and outputting an

instruction to the instruction decoder based on which instruction the fetch unit determines to fetch; and

an address renamer mapping a logical address generated by the instruction decoder for an instruction into a real address of a memory device in an execution unit.

13. A method of fetching instructions for processing in a multi-threaded processor, comprising:

receiving, at a fetch unit of a processing pipeline, information from at least one other stage of the processing pipeline, the processing pipeline including a number of stages, each stage processing at least one instruction, each instruction belonging to one of a plurality of threads;

first determining a processing time of the processing pipeline occupied by each thread based on the received information; and

second determining from which thread to fetch an instruction for processing by the processing pipeline based on the determined processing time for each thread.

14. The processor of claim 13, wherein the second determining step determines the thread having the smallest determined processing time as the thread from which to fetch an instruction for processing.

15. The processor of claim 13, wherein the received information includes the operation type of instructions in the processing pipeline.

16. The processor of claim 15, wherein the received information further includes the operation type of instruction leaving the processing pipeline.

17. The processor of claim 16, wherein the first determining step comprises:

incrementing, for each thread, a counter associated with the thread by a processing time associated with each instruction of the associated thread in the processing pipeline; and

decrementing, for each thread, the counter associated with the thread by a processing time associated with each instruction of the associated thread leaving the processing pipeline.

18. The processor of claim 17, wherein the second determining step determines the thread associated with the counter having a smallest count value as the thread from which to fetch an instruction for processing.

19. The processor of claim 13, wherein the first determining step generates a weighted instruction count for each thread as the determined processing time of each thread, the weighted instruction count for a thread is a count of the instructions for the thread in the processing pipeline with each

instruction weighted by the cycle counts associated with processing the instruction.

20. The processor of claim 19, wherein the first determining step comprises:

incrementing, for each thread, a counter associated with the thread by the cycle counts associated with each instruction of the associated thread in the processing pipeline; and

decrementing, for each thread, the counter associated with the thread by the cycle counts associated with each instruction of the associated thread leaving the processing pipeline.

21. The processor of claim 20, wherein the second determining step determines the thread associated with the counter having a smallest count value as the thread from which to fetch an instruction for processing.